

FIG. 1

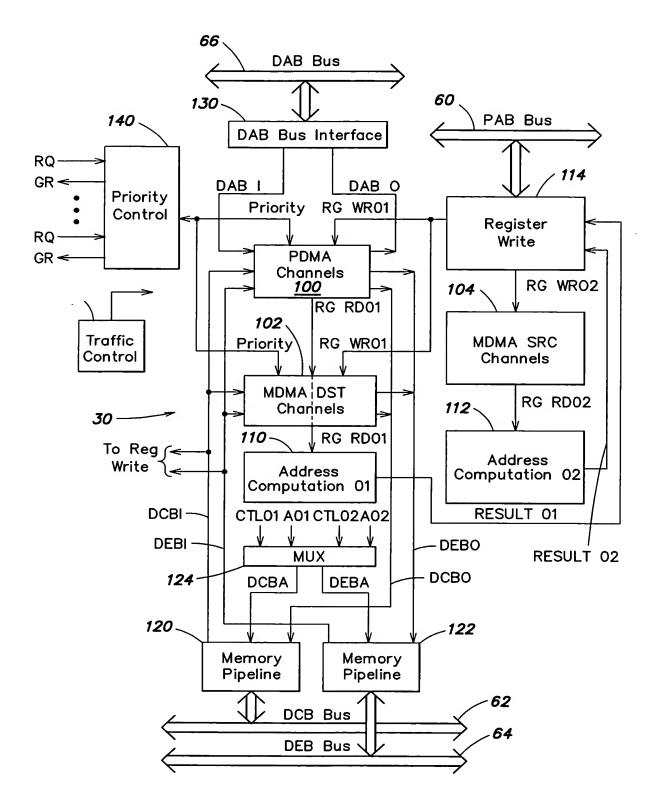


FIG. 2

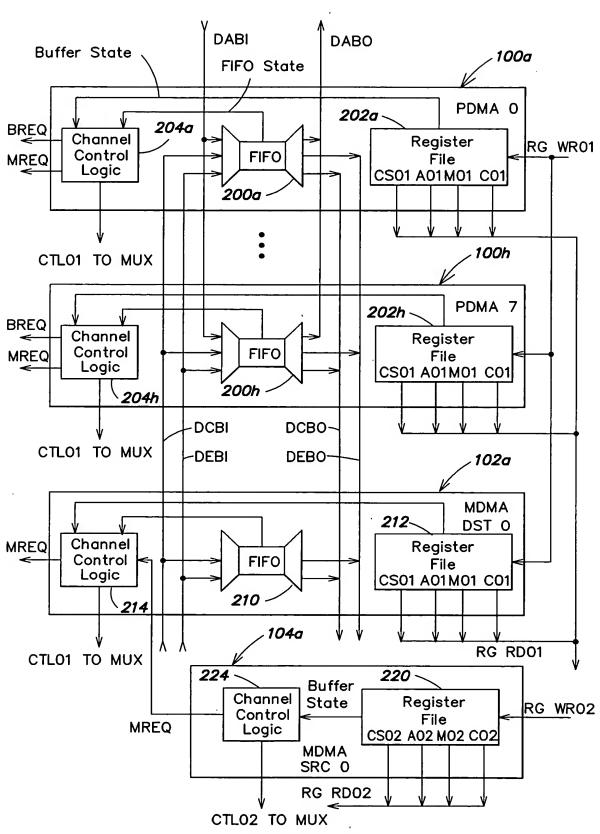
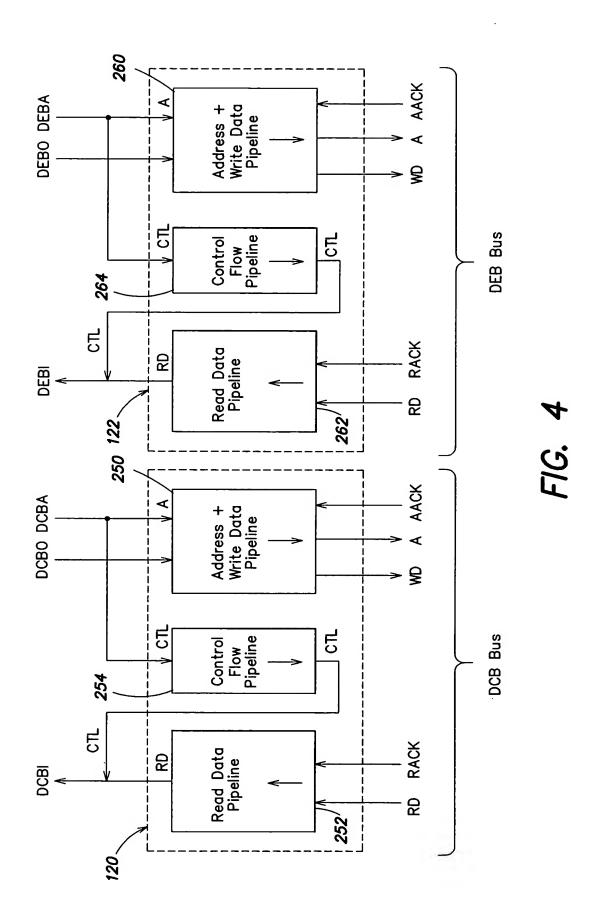


FIG. 3

DMA Controller Having Programmable Channel Priority Hayden et al. Serial No.: 10/786,853



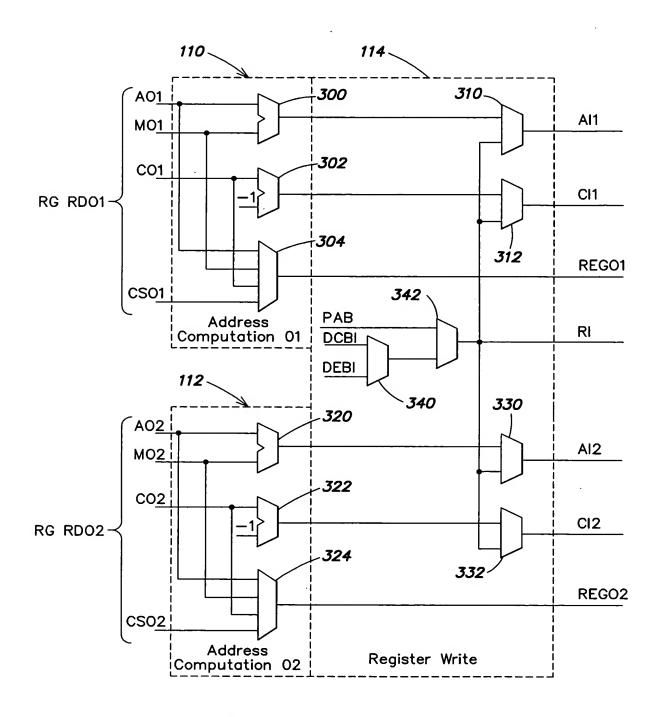
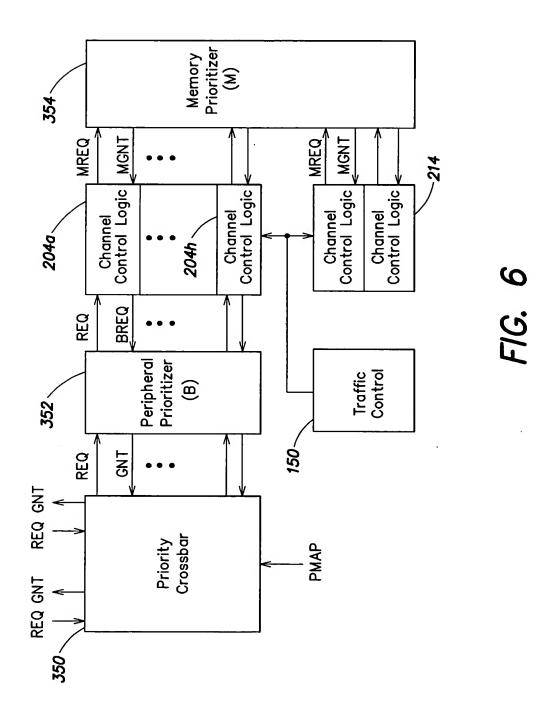
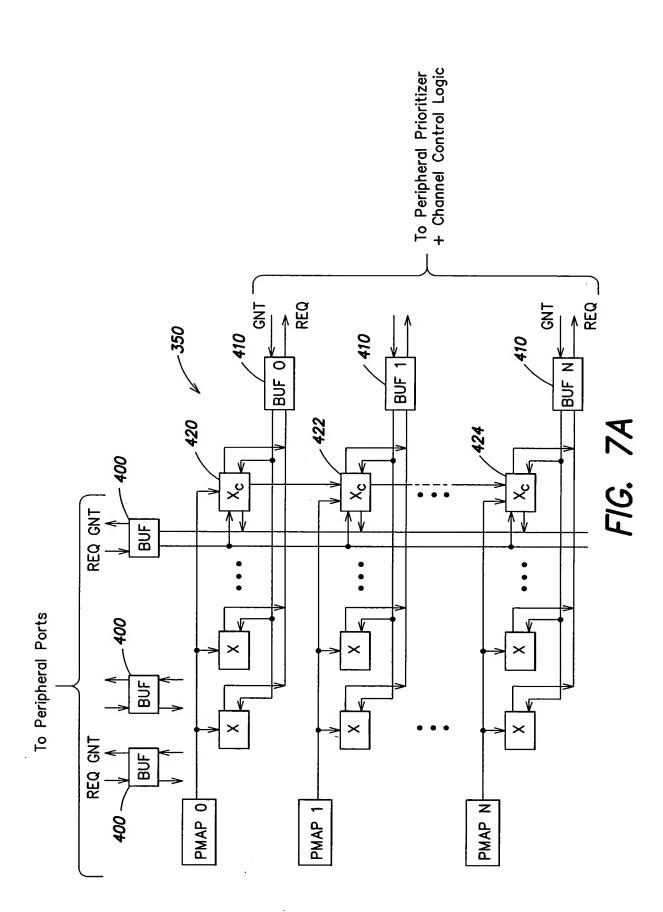


FIG. 5

DMA Controller Having Programmable Channel Priority Hayden et al. Serial No.: 10/786,853





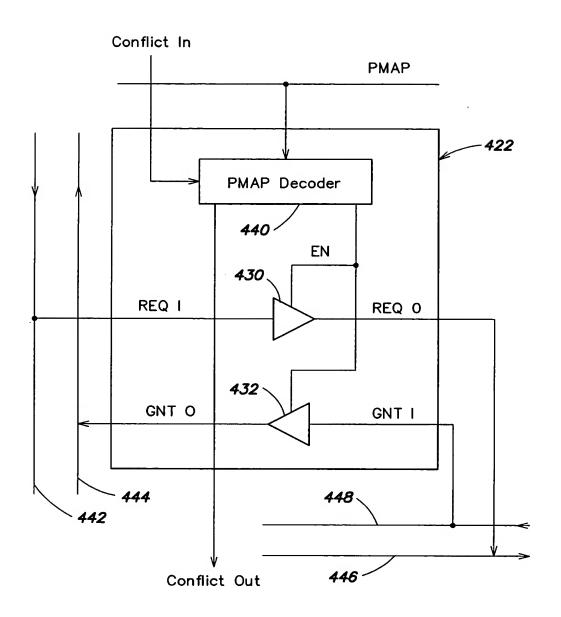
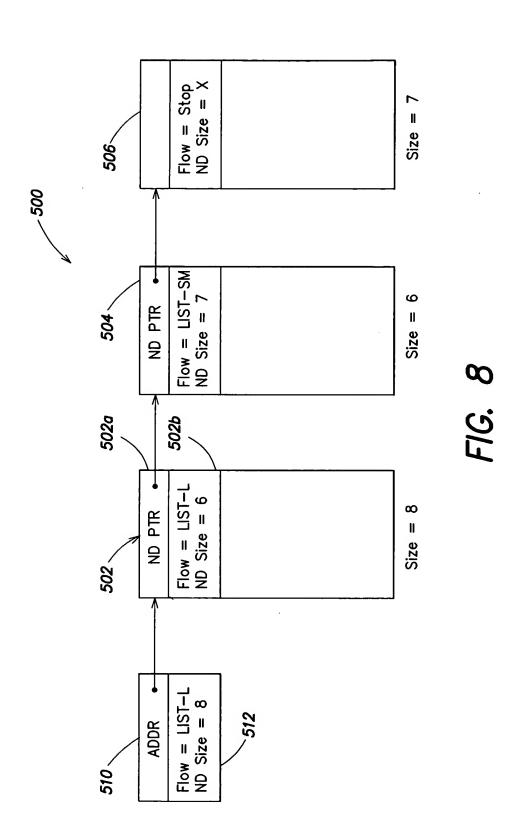


FIG. 7B

DMA Controller Having Programmable Channel Priority Hayden et al. Serial No.: 10/786,853



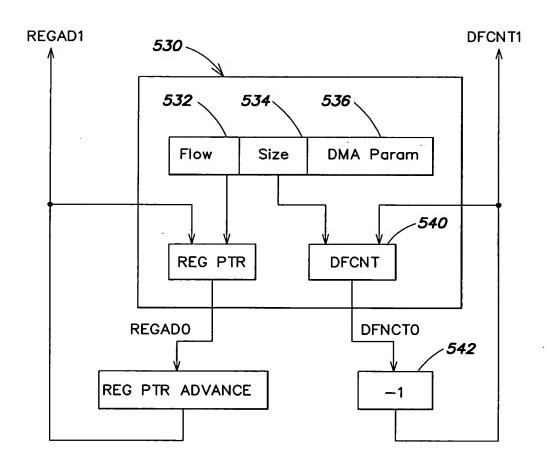
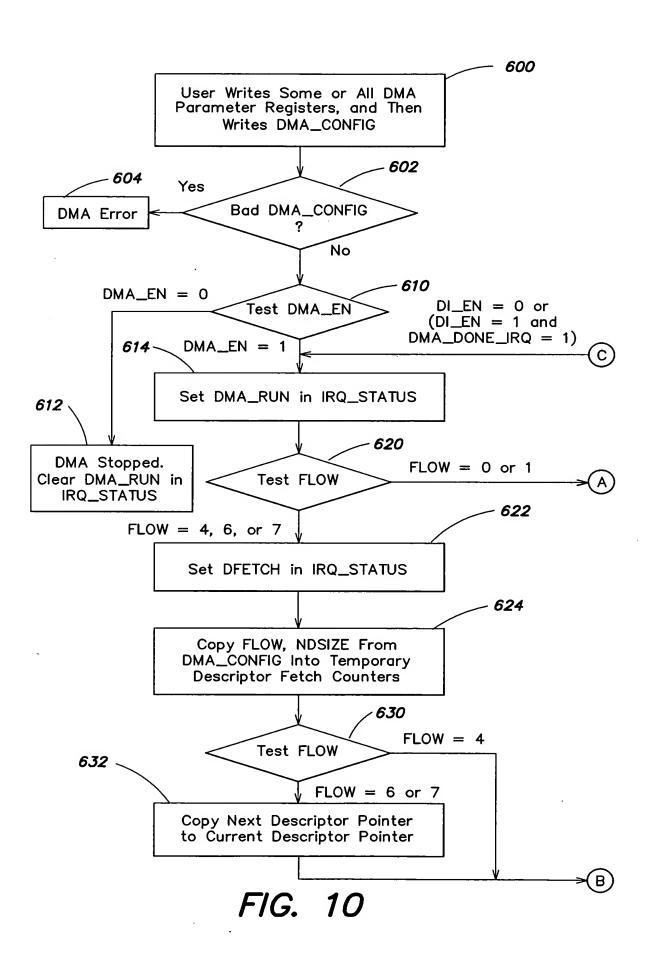


FIG. 9



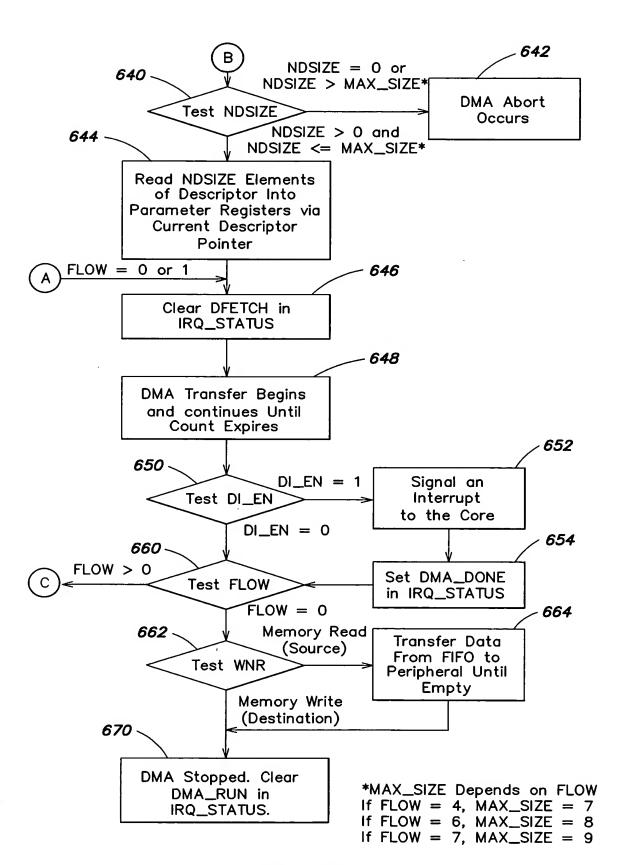


FIG. 11